Non-Intrusive Detection of Defects in Mixed-Signal Integrated Circuits Using Light Activation

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***Abstract*—The quality level of mixed-signal ICs lags behind the below-part-per-million defect test escape rates of digital ICs, as a result of the traditional testing based on performance specifications. Methods increasing the controllability to solve the problem of the low fault coverage of analog and mixed-signal circuits are in practice limited due to the excessive area overhead they require and their impact on the normal circuit operation. This paper presents a non-intrusive method to improve the controllability using light as an activation mechanism. The necessary simulation models are introduced to use the proposed method in the context of a defect-oriented test approach. This work also describes a workflow which enables the application of the method to large-scale industrial circuits. Finally, effective results are shown on an industrial mixed-signal front-end circuit under test (CUT) demonstrating around 27% increase in the number of detectable defects.**

I. Introduction

The quality requirements of mixed-signal ICs have been increasing tremendously over the years, as the number of chips in new systems, such as self-driving cars, has been rising constantly [1]. On the other hand, the quality limitations of today's mixed-signal ICs are predominantly determined by the analog part, because of the high analog test escape rates. The reason is that the digital part is tested by well-defined structural tests for quite some time now, whereas the analog blocks are traditionally tested according to functional specifications. This rather empirical approach results in long and expensive test sets which cause analog testing to dominate the testing effort and cost for mixed-signal ICs. Furthermore, these specification-based tests often lead to poor fault coverage, since the possible defects are not directly addressed in such a methodology [2], [3].

In order to improve the fault coverage in mixed-signal circuits, previous work has mostly focused on increasing the limited observability [4]–[7]. Mapping different analog performances into time-based parameters which can be probed out by a mixed-signal test bus has for example been proposed to measure analog specifications [4]. An automatic method based on injecting small detection blocks into less observable nodes has been proposed in [5]. Moreover, a non-intrusive sensor based approach has been proven to be successful in testing millimeter-wave circuits [6], [7]. The limitation of these methods is generally caused by the lack of sufficient controllability in large-scale mixed-signal circuits.

Methods based on test signal generation have therefore been proposed in order to optimize the available controllability through the primary inputs of analog and mixed-signal circuits [8]–[13]. A hierarchical fault-based approach has been proposed to generate a set of test frequencies which can result in either a maximum fault coverage or a minimum number of frequencies [8]. An ATPG algorithm has been presented to synthesize a test stimulus in order to allow the prediction of circuit specifications [9]. An automatic multi-frequency test generation technique based on graph theory has been proposed in order to construct input signals for detecting catastrophic and parametric defects [10]. A more generalized hierarchical method has been built on this using observability and controllabilty computations [11]. Furthermore, the use of ATPG algorithms has been extended to high-speed analog circuits by [12]. Finally, an ATPG algorithm based on circuit partitioning and interval analysis has been proven to be successful without any limitation on the number of inputs or the non-linearity of the circuit [13]. However, these methods rely only on the available circuit inputs. Therefore, the effectiveness of ATPG based methods is often inadequate for large-scale mixed-signal circuits with only a limited number of primary inputs. Moreover, most of the proposed algorithms have certain assumptions about the type of circuit under test (CUT), such as being linear.

Design for testability (DfT) methods have therefore been proposed in order to overcome the limitations of the above methods based on test signal generation [14]–[18]. Early DfT work has focused on using analog buffers and multiplexers to have extra circuit nodes which gives direct access from outside the chip [14]. The evident disadvantages of this methodology are the large area overhead and the long testing time because of the serial manner of testing. The loading effect introduced by the analog multiplexers and/or buffers also makes this approach almost inapplicable to many analog circuits. A DfT method based on current injection has been proposed to overcome the problem of excessive loading [15]. However, this technique also suffers from large area overhead and long testing time. An oscillation-based approach has been introduced based on re-configuring mixed-signal circuits to start oscillation [16], [17]. The properties of the oscillation, such as the frequency and the amplitude, have been used to detect defective CUT. Methods based on this approach are intrusive and only applicable to a limited set of analog circuits. Finally, a general DfT method has been proposed which is based on modifying the topology of the CUT by connecting internal circuit nodes to the supply or ground [18].

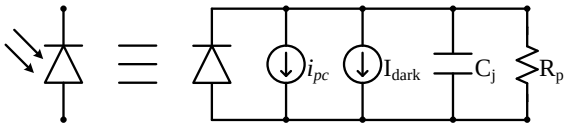


Fig. 1. The symbol and the equivalent circuit model of a photodiode.

This method is also intrusive, since it adds extra parasitic capacitance to internal circuit nodes. Besides, it requires digital control signals to be routed inside the analog part, which is not always preferable.

In this paper, an external non-intrusive controllability technique is proposed which is based on using the effect of light incident on mixed-signal ICs to activate hard-to-detect defects in a parallel manner. Light is used to generate photocurrents in intrinsic silicon diodes which are ubiquitous in every IC. The presence of defects may lead to a totally different behavior when the photocurrents are introduced. The proposed method is non-intrusive, it does not require any area overhead, does not create any loading, yet it increases the fault coverage. The effect of light has been used in order to increase the fault coverage for digital circuits particularly using I_{CCQ} tests [19]. However, the idea of using light as a means of controllability in the context of the defect-oriented approach is a novel method to create test sets for analog and mixed-signal ICs.

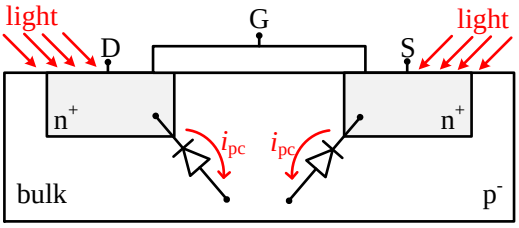
The paper is organized as follows. In Section II, the theory behind the proposed approach and the proposed simulation models will be explained in detail. Measurement results confirming the proposed models and fault simulation examples demonstrating the potential of the proposed method will be presented in Section III. The photosim workflow, which enables the application of the proposed method to large-scale circuits, will be explained in Section IV. In Section V, an industrial case study will be presented, which demonstrates the effectiveness of the proposed method and the photosim workflow. Conclusions will be drawn in Section VI.

II. Theory and Simulation Models

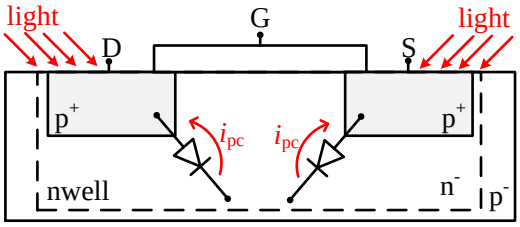
In order to explain the basic theory and the proposed methodology, it is important to first analyze the behavior of a photodiode. The proposed method and the simulation models are explained on that basis later.

A. Basic Photodiode Theory

A photodiode is a p-n junction in which electron-hole pairs are created when a photon is incident, provided that the energy of the photon is larger than the semiconductor bandgap [20]. Fig. 1 shows the symbol and the equivalent circuit model of a typical semiconductor photodiode, where the diode in the equivalent model is an ideal one. The junction capacitance C_j and the shunt resistance R_p are connected in parallel to this ideal diode. The current source that models the small amount of current even when no light is present, is indicated as I_{dark}. The light-induced current source i_{pc} is also shown in Fig. 1.



(a)



(b)

Fig. 2. Cross-section of (a) an n-channel and (b) a p-channel transistor, demonstrating the intrinsic junction diodes and the effect of incident light.

The direction of both I_{dark} and i_{pc} are in the opposite direction of the current flow of a forward biased diode. This is because when the absorption of the light occurs, the holes move toward the anode and the electrons move toward the cathode, which then produces the photocurrent. Therefore, the total output current of a photodiode I_{PD} is the summation of the dark current and of the light-induced current:

$$I_{PD} = I_{dark} + i_{pc} \tag{1}$$

The dark current, which includes the photocurrent generated by background radiation and the saturation current of the semiconductor junction, can be neglected because of its small magnitude and its existence even under normal conditions of the ICs as well. The light-induced current i_{pc}, on the other hand, depends on the intensity of the incident light and the responsivity of the semiconductor at its wavelength, and can be expressed as:

$$i_{pc} = P_{light} \times R(\lambda) \tag{2}$$

where P_{light} is the power of the incident light at a certain wavelength and $R(\lambda)$ is the spectral responsivity having the unit of A/W. The wavelength dependence of the photocurrent can also be represented as the ratio of the number of carriers to the number of incident photons, which is unitless.

In conclusion, any p-n junction can behave as a photodiode, which means that a significant amount of current can be induced in the presence of incident light. The magnitude of this induced current is proportional to the power and the spectrum of the light source and the properties of the junction, e.g. area, doping, material type.

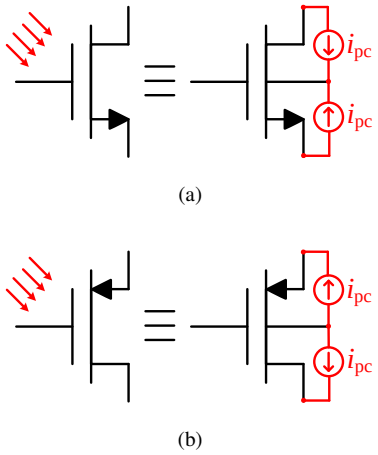


Fig. 3. Compact simulation models for (a) n-channel and (b) p-channel transistors including the effect of light.

B. Proposed Methodology

The basic concept of the proposed method is based on the physical phenomenon that when the light is incident on a die surface, the existing junctions behave as photodiodes. Since the light can be incident everywhere on a die, a huge number of photodiodes are activated at the same time. The structures of these photodiodes in CMOS processes are shown in the cross-section of n-channel and p-channel transistors in Fig. 2. When photons are absorbed by an n-channel transistor, light-induced currents start to flow from source to bulk and drain to bulk as shown in Fig. 2(a). The directions of the light-induced currents for a p-channel transistor, on the other hand, are from bulk to source and bulk to drain as shown in Fig. 2(b).

The proposed method relies on using light as an activation mechanism in order to reveal defects in ICs due to the effect of the generated light-induced currents. The behavior of a defect-free CUT is not significantly affected by the photocurrents, since those are much smaller than the nominal currents in the branches. However, at the existence of a defect that creates a high impedance node, e.g. an open track or via, or a transistor with a gate to source short in the CUT, the photocurrents around the affected node can easily pull the node away from the normal biasing voltage and hence create a detectable change in the behavior of the CUT. It is important to note that light isolation during wafer probing traditionally is a prerequisite in analog and mixed-signal testing in order to avoid the disturbance of sensitive measurements. Therefore, the idea of using light as a means of controllability in the context of the defect-oriented approach is a novel method to create test sets for analog and mixed-signal ICs.

C. Simulation Models

In order to create tests and/or to evaluate the efficacy of those tests a simulation model is required, which accounts for the effect of the light in analog and mixed-signal ICs. The model is preferred to be compatible with fault simulations and to be compact so that the use of common transistor models is enabled. In addition, the model should adequately represent the equivalent circuit model of a photodiode as in Fig. 1.

The simulation model used satisfies these requirements for n-channel and p-channel transistors as demonstrated in Fig. 3. The ideal diode and the elements modeling the nonidealities, i.e. the junction capacitance C_j and the shunt resistance R_p, are not included in the proposed model since these are taken into account by the standard transistor models. The current source which models the contribution of the dark current is also discarded, because the magnitude of this current is small. Another reason is that this small current already exists during the traditional testing and/or during the normal operation of the IC, therefore it is not required for test generation or evaluation purposes.

The model used includes two current sources between the bulk node and the source node or the drain node for every transistor, which models the effect of the light-induced currents i_{pc}. The direction of the current flow is correctly modelled for n-channel and p-channel transistors as indicated in Fig. 3(a) and (b). These current sources can be injected automatically by the photosim workflow as will be explained in Section IV. In Section III the validity of the simulation models is proven by the measurement results from fabricated silicon, and the efficacy in increasing the controllability of defects is demonstrated by fault simulation examples.

III. Measurement and Simulation Results

Fig. 4 shows the schematic of the test circuit which is used to validate the proposed models. It is a folded-cascode amplifier circuit with class-AB output stage, which is a common building block in analog and mixed-signal ICs. For measurement purposes, it is configured as a unity-gain buffer by internal negative feedback. Fig. 4 also indicates the location of the injected defect 1 in the circuit schematic. Defect 1 is injected by intentionally creating a small gap in a metal track.

Fig. 5 shows the test chip which has been fabricated in 0.35μm BCD technology including one defect-free version and intentionally defective versions of the test circuit [21]. Both circuits share the same input signal, supply line and bias current, whereas each circuit has an individual output pin in order to prevent possible loading effects that might be introduced by serializing measurement methods. Due to the presence of the defect-free version of the circuit on the same die, it is possible to analyze the effect of the process variations and to asses a testing approach by comparing the defect-free results with the defective ones.

Fig. 6 shows the results of the DC characterization and the fault simulations for defect 1 in comparison with the measurement results of the good circuit. In order to introduce the least possible loading effects, especially for the defective circuits, the output voltages are measured across the terminals of a true current source which is configured to conduct zero current. A previously verified fault model for open defects is used in the fault simulations [21]. This model is based on injecting a high-value resistance between the affected nodes to model the small amount of leakage current. The use of a range

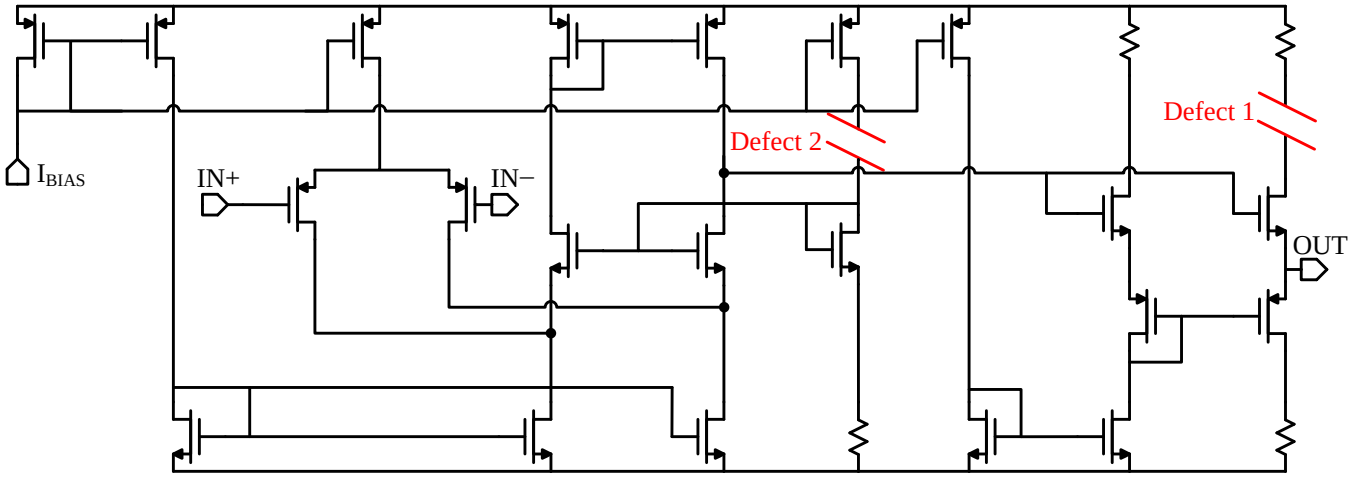


Fig. 4. Schematic of the measured and simulated defective analog buffer circuit.

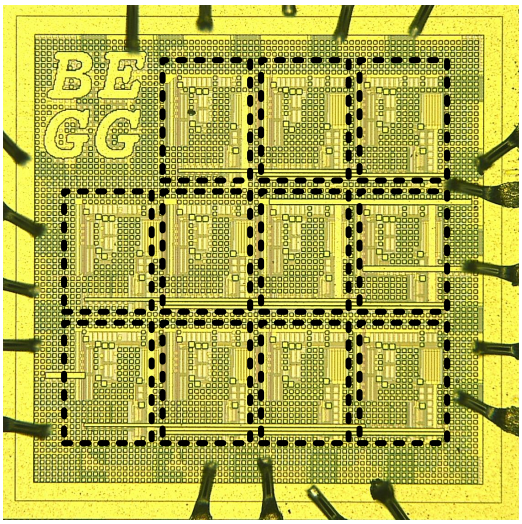


Fig. 5. Die micrograph of the produced test chip.

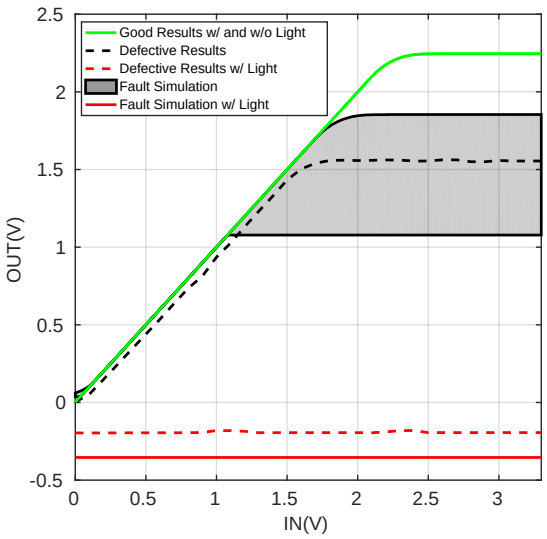


Fig. 6. Measurement results compared to simulation results for the good circuit and for the circuit including defect 1 in dark and with light conditions.

of values for the resistance is also adopted here since it gives more accurate results as proven by the agreement between the fault simulation and the defective measurement results in Fig. 6.

The consistency of the measurement results for light and dark conditions for the good circuit proves the assumption that a defect-free circuit is not significantly affected by the photocurrents, since those are much smaller than the nominal currents in the branches. The simulation results for the good circuit are omitted from Fig. 6 for the sake of simplicity as those precisely match the measurement results in both conditions.

The measurement result of the circuit with defect 1 in the presence of light is also shown in Fig. 6. In order to measure the effect of light on the test circuit, the measurements have been carried out on a bare die without any insulating cover. The significant change at the output of the defective circuit shows the extent of the effect of light on analog and mixed-signal circuits. The choice of the defect location also enables to interpret this effect independently of other factors, since the defect is injected right on the output branch.

The result of the fault simulation with light for defect 1 is also shown in Fig. 6. This simulation includes both the fault model for an open defect and the proposed models accounting for the effect of light on transistors. The current sources included in the model have been injected automatically to every transistor using the photosim workflow, which will be described in Section IV. The agreement between the measurement results (red dashed line) and the fault simulation (red solid line) in Fig. 6 strongly confirms the validity of the proposed model. Moreover, accurate fault simulations in the presence of light enables creating tests using light to increase controllability and evaluating the fault coverage of those tests. The efficiency of light in defect activation can be observed as

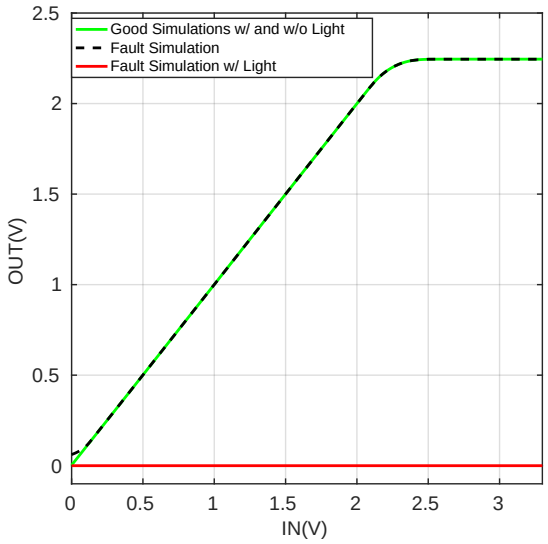


Fig. 7. Fault simulation results for defect 2 compared to the good circuit with and without light.

the defect 1 becomes easily detectable in the presence of light, whereas it is a hard-to-cover defect in traditional dark tests.

Defect 2, shown in Fig. 4, is another example in which light can effectively be used to enable the detection of a defective circuit. Defect 2 is an open defect on a biasing branch which is not easy to detect as demonstrated by the fault simulation result in Fig. 7. This is because the defective CUT satisfies the specifications in DC conditions although the biasing of the cascode transistors is degraded. This defect can however easily be detected when light is incident on the chip as shown by the fault simulation result with light in Fig. 7. These fault simulations have been carried out by the Photosim workflow similar to the case of defect 1. Since the light-induced currents cancel out the small amount of leakage currents, which allows the operation of the cascode transistors in DC conditions, the output of the CUT is entirely pulled down to ground. Therefore, the detection of defect 2 can be straightforward when light is used as an activation mechanism.

The proposed method increases controllability fully in parallel. This can be proven by the fact that defect 1 and defect 2 can be activated simultaneously by using light with the same test setup, i.e. using the same input signal and probing the same output node. Moreover, the proposed method is absolutely non-intrusive, since it is not required to modify or extend the original architecture of the folded-cascode amplifier. In other words, the use of light is an external controllability method which is, therefore, superior to traditional methods offering increased controllability in terms of area overhead and impact on the normal circuit operation. The efficacy of the method in a large-scale industrial mixed-signal circuit will further be evaluated with a case study in Section V.

IV. Photosim Workflow

A unified simulation workflow called Photosim is implemented in order to cope efficiently with modeling the effect of

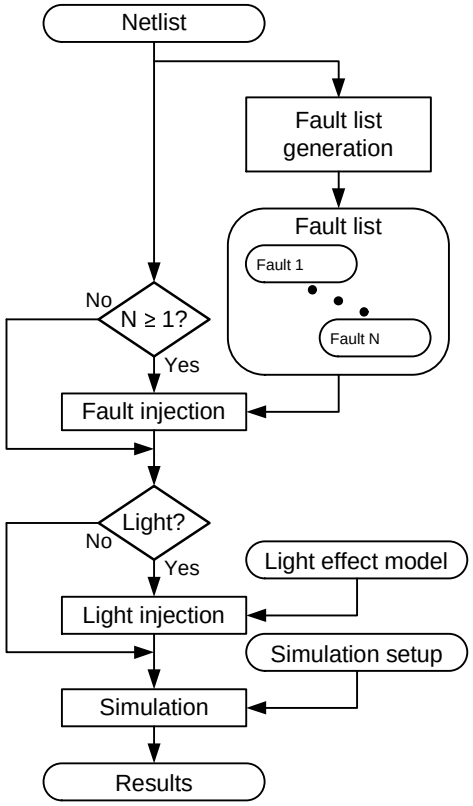


Fig. 8. Photosim workflow.

light on a large-scale circuit where many defects are possible. It is a simulation tool that can handle large circuits in an automated way.

The flow chart of Photosim is shown in Fig. 8. The tool requires a circuit netlist, a fault setup, a light effect model and a simulation setup as inputs. The type and the number of faults to be considered are specified by the user. Within the scope of this work faults from the 5-fault model for CMOS transistors are considered, which contains 3 short circuits (gate-source, gate-drain, drain-source) and 2 open circuits (open drain, open source). The model for the effect of light has been explained in Section II.

In the first step, the list of possible faults is generated in order to inject those into the circuit netlist. It is also possible to only allow a subset of these faults to be injected, which reduces the simulation time when only that subset is of interest, e.g. only the short circuit defects, or all the defects from a single transistor. Furthermore, it is also possible to exclude the fault injection step in order to only simulate the good circuit.

The second step consists of injecting the photodiode effect into the circuit. If desired, the injection of this effect can also be skipped. This allows the comparison of testing with or without the effect of light.

In the last step the results of the simulations are generated. The type of these simulations are specified by the simulation setup which is user input. The output of the Photosim is typically the fault coverage values of the test sets, which are

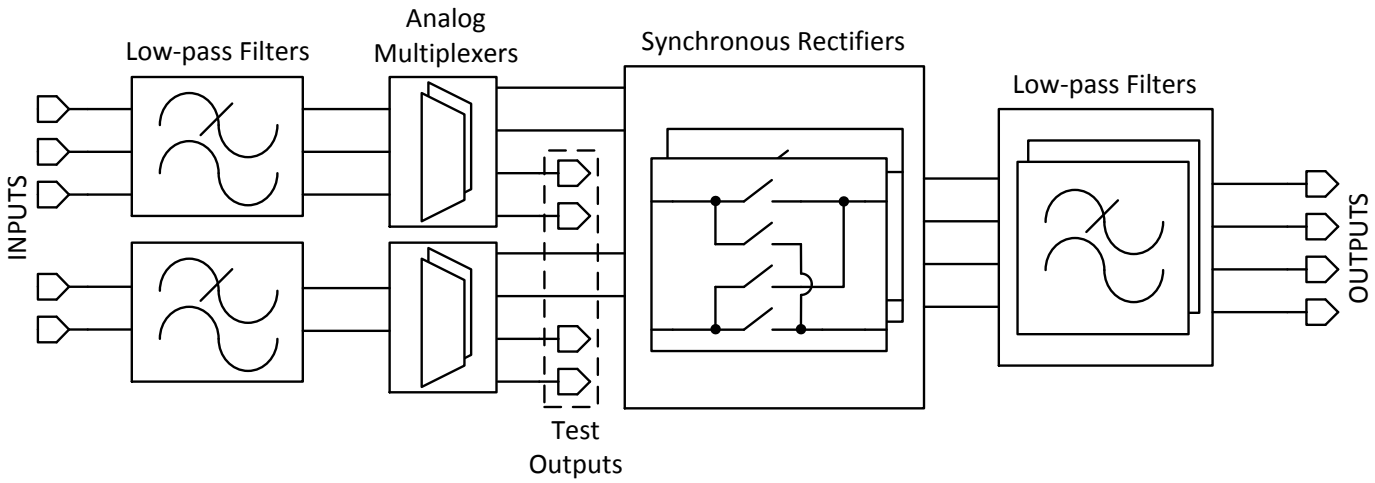


Fig. 9. Block diagram of the industrial mixed-signal front-end circuit used as a case study.

described by the simulation setup.

V. Industrial Case Study

In order to demonstrate the efficacy and the scalability of the proposed method, it has been applied to an industrial mixed-signal front-end circuit which includes low-pass filters, analog multiplexers, and synchronous rectifiers, as shown in Fig. 9. The DC correcting blocks employed by this front-end circuit are omitted from Fig. 9 for the sake of simplicity. This circuit is part of a commercial automotive product which is implemented in 0.35μm BCD technology. It is a large-scale block which involves in total 335 transistors. While the observability is only available through the test outputs of the analog multiplexers shown in Fig. 9. The controllability of the circuit is also very limited, since the number of accessible inputs is small compared to the overall number of elements in the circuitry.

Eight different test configurations, which are employed by the production line testing of this block, have been evaluated in terms of the number of detected defects. These test configurations involves activating different analog paths and measuring either the on-resistances or the leakage currents. The evaluation has been carried out using the Photosim workflow explained in Section IV. Each test configuration from the selected set of eight has been implemented as a simulation setup. These simulation setups, together with the circuit netlist, have been given as input to Photosim. The standard 5-fault model for CMOS transistors has been used in fault list generation step. The results of the fault simulations have been compared with the detection limits of every test configuration in order to decide if a defect can be detected by that configuration. The simulation results of the good circuit including the effect of light have been also monitored for every configuration in order to confirm the validity of the detection limits. In this way the number of detectable defects has been calculated for each configuration both in light and in dark conditions.

TABLE I
Results of the Case Study

Configuration	Detected **without Light**	Detected **with Light**	Total
1	172	201	201
2	172	201	201
3	124	140	140
4	98	111	111
5	204	253	253
6,7,8	185	259	262
Overall	675	859	862

Table I summarizes the evaluation results of the selected eight test configurations. Each row demonstrates the number of detected defects by each test configuration with light, without light and with the combination of the two as well. The results of the test configurations 6, 7, and 8 are reported together, since those test configurations require the results of each other. The overall number of detected defects is shown in the last row which takes the redundancy among different configurations into account. The effectiveness of light as a defect activation mechanism is proven by the consistent increase in the number of detectable defects for every configuration. The achieved increase in the overall detection is around 27%, i.e. from 675 defects upto 859 defects.

Another important conclusion is that the number of detected defects by only using light tests is almost equal to the total number of detectable defects. The extra detectability offered by dark tests is only limited to three defects which are all from the combination of the last three configurations. Therefore, applying only the tests using light for increased controllability might be sufficient in many cases. This allows avoiding an excessive increase in test time and cost which is a major

contributor to the cost of mixed-signal ICs.

VI. Conclusion

A non-intrusive controllability method for analog and mixed signal circuits has been proposed, which is based on using light as an external activation mechanism. The proposed method is fully parallel, since the effect of incident light can simultaneously be everywhere on a silicon die. It is preferable above traditional methods offering increased controllability, which rely on modifying or extending the architecture of the CUT, in terms of area overhead and impact on the normal operation of the CUT. In addition, the necessary compact simulation models have been introduced to use the proposed method in the context of a defect-oriented approach. These models have been validated by the measurement results of an experimental test chip fabricated in 0.35μm BCD technology. A unified workflow called Photosim has been implemented, which involves both fault simulation and modeling the effect of light on transistors. This tool has successfully been applied to large-scale mixed-signal circuits.

The proposed method has then been applied to a large-scale industrial front-end circuit which is a part of a commercial automotive product. This mixed-signal front-end circuit consists of 335 transistors. This case study has demonstrated around 27% increase in the number of detectable defects for the selected eight test configurations implemented in production line testing. These results have also shown that the use of only light testing might be sufficient in many cases which avoids an excessive increase in test time.

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References

[1] W. Dobbelaere, R. Vanhooren, A. Coyette, and G. Gielen, "Analog fault coverage improvement using defect-specific masking," *VOICE*, 2014.

[2] W. Dobbelaere, R. Vanhooren, W. D. Man, K. Matthijs, A. Coyette, B. Esen, and G. Gielen, "Analog fault coverage improvement using final-test dynamic part average testing," *2016 IEEE International Test Conference (ITC)*, pp. 1–9, Nov 2016.

[3] G. Gielen, W. Dobbelaere, R. Vanhooren, A. Coyette, and B. Esen, "Design and test of analog circuits towards sub-ppm level," *2014 International Test Conference*, pp. 1–2, Oct 2014.

[4] S. Sunter and A. Roy, "A mixed-signal test bus and analog bist with 'unlimited' time and voltage resolution," *2011 Sixteenth IEEE European Test Symposium*, pp. 81–86, May 2011.

[5] A. Coyette, B. Esen, R. Vanhooren, W. Dobbelaere, and G. Gielen, "Automatic generation of autonomous built-in observability structures for analog circuits," *2015 20th IEEE European Test Symposium (ETS)*, pp. 1–6, May 2015.

[6] L. Abdallah, H. G. Stratigopoulos, S. Mir, and J. Altet, "Defect-oriented non-intrusive rf test using on-chip temperature sensors," *2013 IEEE 31st VLSI Test Symposium (VTS)*, pp. 1–6, April 2013.

[7] A. Dimakos, H. G. Stratigopoulos, A. Siligaris, S. Mir, and E. D. Foucauld, "Built-in test of millimeter-wave circuits based on non-intrusive sensors," *2016 Design, Automation Test in Europe Conference Exhibition (DATE)*, pp. 505–510, March 2016.

[8] N. Nagi, A. Chatterjee, A. Balivada, and J. A. Abraham, "Fault-based automatic test generator for linear analog circuits," *Proceedings of 1993 International Conference on Computer Aided Design (ICCAD)*, pp. 88–91, Nov 1993.

[9] R. Voorakaranam and A. Chatterjee, "Test generation for accurate prediction of analog specifications," *Proceedings 18th IEEE VLSI Test Symposium*, pp. 137–142, 2000.

[10] S. D. Huynh, S. Kim, M. Soma, and J. Zhang, "Automatic analog test signal generation using multifrequency analysis," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 5, pp. 565–576, May 1999.

[11] M. Soma, S. Huynh, J. Zhang, S. Kim, and G. Devarayanadurg, "Hierarchical atpg for analog circuits and systems," *IEEE Design Test of Computers*, vol. 18, no. 1, pp. 72–81, Jan 2001.

[12] R. Voorakaranam, S. S. Akbay, S. Bhattacharya, S. Cherubal, and A. Chatterjee, "Signature testing of analog and rf circuits: Algorithms and methodology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 5, pp. 1018–1031, May 2007.

[13] A. Coyette, B. Esen, W. Dobbelaere, R. Vanhooren, and G. Gielen, "Automatic test signal generation for mixed-signal integrated circuits using circuit partitioning and interval analysis," *2016 IEEE International Test Conference (ITC)*, pp. 1–10, Nov 2016.

[14] M. Jarwala and S. J. Tsai, "A framework for design for testability of mixed analog/digital circuits," *Proceedings of the IEEE 1991 Custom Integrated Circuits Conference*, pp. 13.5/1–13.5/4, May 1991.

[15] J. Velasco-Medina, T. Calin, and M. Nicolaidis, "Fault detection for linear analog circuits using current injection," *Proceedings Design, Automation and Test in Europe*, pp. 987–988, Feb 1998.

[16] K. Arabi and B. Kaminska, "Oscillation built-in self test (obist) scheme for functional and structural testing of analog and mixed-signal integrated circuits," *Proceedings International Test Conference 1997*, pp. 786–795, Nov 1997.

[17] G. Huertas, D. Vazquez, E. J. Peralias, A. Rueda, and J. L. Huertas, "Testing mixed-signal cores: a practical oscillation-based test in an analog macrocell," *IEEE Design Test of Computers*, vol. 19, no. 6, pp. 73–82, Nov 2002.

[18] A. Coyette, B. Esen, R. Vanhooren, W. Dobbelaere, and G. Gielen, "Automated testing of mixed-signal integrated circuits by topology modification," *2015 IEEE 33rd VLSI Test Symposium (VTS)*, pp. 1–6, April 2015.

[19] M. Smayling, "Method and system for fault testing integrated circuits using a light source," *US Patent 5,420,522*, May 30 1995.

[20] F. Tavernier and M. Steyaert, *High-speed optical receivers with integrated photodiode in nanoscale CMOS*. Springer, 2011.

[21] B. Esen, A. Coyette, W. Dobbelaere, R. Vanhooren, and G. Gielen, "Effective dc fault models and testing approach for open defects in analog circuits," *2016 IEEE International Test Conference (ITC)*, pp. 1–9, Nov 2016.